## **CLAIMS:**

1. A communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences;

circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry for selecting a bit loading sequence with a lowest error rate.

- 2. The communication system according to claim 1, wherein the plurality of channels comprises independent logical channels decomposed from a Multiple-Input, Multiple-Output channel.
- 3. The communication system according to claim 1, wherein the plurality of channels comprises independent logical channels decomposed from an orthogonal frequency division multiplexing channel.
- 4. The communication system according to claim 1, wherein the plurality of modulation alphabets is capable of representing data using a different number of bits.
- 5. The communication system according to claim 4, wherein for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded on at least one channel of the plurality of channels.
- 6. The communication system according to claim 5, wherein the fixed data rate is selected based on a channel quality indicator.
- 7. The communication system according to claim 6, wherein the channel quality indicator is calculated at the transmitter.

- 8. The communication system according to claim 6, wherein the channel quality indicator is calculated at the receiver.
- 9. The communication system according to claim 1, wherein the determined power allocation provides a power weighting for at least one channel of the plurality of channels.
- 10. The communication system according to claim 9, wherein if an identical modulation alphabet is used for at least two logical channels then a greater power weighting is allocated to weaker logical channels.
- 11. The communication system according to claim 1, wherein a power allocation used to transfer the data comprises the power allocation determined for the at least one bit loading sequence.
- 12. The communication system according to claim 1, wherein the transmitter comprises a plurality of transmitting antennas.
- 13. The communication system according to claim 1, wherein the receiver comprises a plurality of receiving antennas.
- 14. The communication system according to claim 1, further comprising coding circuitry for adding parity bits to system bits and for distinguishing between the parity bits and the system bits.
- 15. The communication system according to claim 14, wherein the parity bits are transferred on a weak channel.
- 16. The communication system according to claim 14, wherein for a bit loading sequence having an identical modulation alphabet on at least two

channels of the plurality of channels, the parity bits are transferred on at least one of a weakest channel and the power allocation is reduced.

- 17. A system according to claim 14, wherein for a bit loading sequence having different modulation alphabets on the plurality of channels, the parity bits are transferred in a least significant bits of a modulation alphabet used on a strong channel.
- 18. A method for transferring data between a transmitter and receiver over a communication channel, the method comprising:

identifying a set of bit loading sequences from a plurality of modulation alphabets;

determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel.

- 19. A communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising:
- a first circuitry means for decomposing a communication channel into a plurality of logical channels;

modulation circuitry having a plurality of modulation alphabets, at least two modulation alphabets are capable of representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels;

a second circuitry means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences; and

a third circuitry for choosing a bit loading sequence having a minimum bit error rate.

20. A method for transferring data between a transmitter and receiver over a communication channel, the method comprising:

decomposing a communication channel into a plurality of logical channels;

selecting from a plurality of modulation alphabets, wherein at least two modulation alphabets for modulating data are capable of representing the data using a different number of bits;

identifying a set of bit loading sequences for a fixed data rate which specify a number of bits to be loaded onto corresponding logical channels of the plurality of channels;

allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences; and

choosing a bit loading sequence having a minimum bit error rate.

- 21. A method according to claim 20, wherein the data to be transferred comprises systematic bits and parity bits, and wherein the parity bits are loaded onto weaker logical channels.
- 22. A communication system for transferring data between a transmitter and receiver over a communication channel, the system comprising:

decomposing means for decomposing a communication channel into a plurality of logical channels;

representing means for representing data using a different number of bits so that for a fixed data rate a set of bit loading sequences is identified which specify a number of bits to be loaded onto corresponding logical channels; allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences; and

choosing means for choosing a bit loading sequence having a minimum bit error rate.

23. A communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

providing means for providing a modulation circuitry having a plurality of modulation alphabets and for providing a set of bit loading sequences;

determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

selecting means for selecting a bit loading sequence with a lowest error rate.